IP core

An IP (intellectual property) core is a block of logic or data that is used in making a field programmable gate array (FPGA) or application-specific integrated circuit (ASIC) for a product. As essential elements of design reuse, IP cores are part of the growing electronic design automation (EDA) industry trend towards repeated use of previously designed components. Ideally, an IP core should be entirely portable - that is, able to easily be inserted into any vendor technology or design methodology. Universal Asynchronous Receiver/Transmitter (UARTs), central processing units (CPUs), Ethernet controllers, and PCI interfaces are all examples of IP cores.

IP cores fall into one of three categories: *hard cores*, *firm cores*, or *soft cores*. Hard cores are physical manifestations of the IP design. These are best for plug-and-play applications, and are less portable and flexible than the other two types of cores. Like the hard cores, firm (sometimes called *semi-hard*) cores also carry placement data but are configurable to various applications. The most flexible of the three, soft cores exist either as a *netlist* (a list of the logic gates and associated interconnections making up an integrated circuit) or hardware description language (HDL) code.

A number of organizations, such as the Free IP Project and Open Cores, have formed to promote open sharing of IP cores.

Read more about it:

>> EETimes has an article, "Early users of IP cores could gain an edge from design reuse."